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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/535,698 | 05/19/2005 | Martin Daum | CH02 0036 US | 9253 |

65913 7590 01/14/2008

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| EXAMINER | |
|---|---|
| MA, CALVIN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 01/14/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/535,698 | DAUM ET AL. | |
| | Examiner | Art Unit | |
| | Calvin C. Ma | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Claim Objections*

2. Claims 1-7 are objected to because of the following informalities:

The word "characterised" used in claims 1, 6, and 7 is misspelled, it should be spelled characterized. Appropriate correction is required.

In line 6 of claim 7, "when is activated" is grammatically incorrect and lack a subject. The examiner went back to an earlier version of the claim and found the subject of the discussion is line "(Gly+1)". Appropriate correction is required.

Claim 5 is improper since the use of parenthesis is reserved only for character (see MPEP 608.1(M)). Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Eu (US Pub 2002/00833480).

As to claim 1, Eu teaches a LC-Display with n gate drivers (i.e. since 14 gate driving IC is an integrated circuit which must multiplex to address a plurality of display line it can function as multiple gate drivers) and a source drivers (13) for driving a Display with dots arranged in x rows and y columns, the gate driver has several output stages (i.e. GL(N-1), and GL(N)) (see Fig. 2, [0024],[0025]) for driving the gate lines of the display, characterised in that, an additional voltage line is provided, which is coupled to the output stages of the gate driver (i.e. Vgh, Vgl are additional voltage line that is in the discharge circuit which is connected to the gate driver) (see Fig. 2 and 4, [0024], [0025], [0033]).

As to claim 6, Eu teaches method for driving a display with n gate drivers (i.e. since 14 gate driving IC is an integrated circuit which must multiplex to address a plurality of display line it can function as multiple gate drivers) and at least one source driver (13), whereas dots are arranged in x rows and y columns, the gate driver has several output stages for driving gate lines (i.e. GL(N-1), and GL(N)) (see Fig. 2, [0024],[0025]) of the display and a capacitance (i.e. the LC capacitor Clc is connected to the common voltage Vcom) (Fig. 2, [0026]) of the selected gate line is connected to the previous gate line characterised in that, an additional supply line of the output stage for

row is activated when the row is activated (i.e. Vgh, Vgl are additional voltage line that is in the discharge circuit which is connected to the gate driver and is activated through the gate driver) (see Fig. 2 and 4, [0024], [0025], [0033]).

As to claim 7, see discussion of claim 6 above, claim 7 is analyzed to be having the same scope as claim 6 and is rejected on the same ground.

As to claim 2, Eu teaches display as claimed in claim 1, whereas the output stage is provided with a PMOS (M2) and two NMOS transistors (i.e. M1, and one in the gate driver 14) and the PMOS transistor is arranged between the supply line VH (20) and the output of the output stage (GL) (see Fig. 4) and the first NMOS transistor MNI (M1) is arranged between the supply line and the output of the output stage and the second NMOS transistor (i.e. NMOS in gate driver) is arranged between the supply line and the output of the output stage (i.e. since the gate driver 14 can be of NMOS design it is connected to M1 NMOS transistor and M2 PMOS transistor in that the two NMOS transistor must be between the supply line and the output GL since they are situated in between these two points) (see Fig. 2, 4, [0028], [0031]).

As to claim 3, Eu teaches display as claimed in claim 1, whereas the additional supply line is routed over a separate track from VL-potential (i.e. the additional supply route goes to an external discharge circuit 12 therefore must be on a different track) (see Fig. 2).

As to claim 4, Eu teaches display as claimed in claim 1, whereas the track of the supply line Wand the track of the supply line are coupled to the same supply level (i.e. . the supply level track can be interpreted as the overall input lines such as Vgl which is the same supply level) (see Fig. 2, 4, [0028], [0031]).

As to claim 5, Eu teaches display as claimed in claim 1, whereas the track of the supply line and the track of the supply line (VLclean) are connected together in a location where the track impedance to the supply circuit's output is low (i.e. the supply level track can be interpreted as the overall input lines such as Vgl and Vgh which both situate on the location of the discharge circuit 12) (see Fig. 2, 4, [0028], [0031]).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jung et al. (US Patent: 6,417,829) and Park et al. (US Patent: 7,136,040) are cited to teach a similar multi-voltage gate line output LCD system.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is (571)270-1713. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
January 3, 2008

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER